ABSTRACT OF THE DISCLOSURE

A memory cell array of a nonvolatile semiconductor memory device includes a plurality of memory cells disposed in a row direction and a column direction. The memory cell array includes a plurality of word lines. Each of the memory cells includes a source region and a drain region. Each of the memory cells includes a select gate and a word gate which are disposed to face a channel region between the source region and the drain region. Each of the memory cells includes a nonvolatile memory element formed between the word gate and the channel region. The word line drive section includes a plurality of unit word line drive sections. Each of the unit word line driver sections drives two of the word lines connected respectively with two of the word gates adjacent to each other in the column direction.